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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,181	10/08/2003	Tetsunobu Kochi	00862.002469.1	5390

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EXAMINER	
KO, TONY	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,181	KOCHI ET AL.	
	Examiner	Art Unit	
	Tony Ko	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,10,11,14 and 18-20* is/are rejected.

7)☒ Claim(s) *2-9 and 12,13, 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/161,402.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/08/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,10-11, 18-20 are rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art (Figs. 1-4), hence forth will be referred as AAPA.

Regarding claim 1, AAPA discloses (Figs. 1-3) a photoelectric conversion device having a plurality of pixel cells each of which includes a photoelectric conversion element (1), a field effect transistor having a gate area for storing signal charge generated by said photoelectric conversion element and a source-drain path for outputting a signal corresponding to the signal charge stored in the gate, a first power

supply line (15) for supplying electric power to said field effect transistor, and a first switch connected between said field effect transistor and said first power supply line, wherein, when a reset voltage for resetting the gate of said field effect transistor is Vsig0, a threshold voltage of said field effect transistor is Vth, current flowing through said field effect transistor is Ia, a voltage applied via said first power supply line is Vcl, and a series resistance of said first switch is Ron. It is inherent from the circuit that each pixel cell satisfies a condition determined by

Vcl – Ron x Ia > Vsig0 – Vth

AAPS discloses (Page 6, lines 11-13) the prior art operate within the linear, however not for all voltages, the disclosed prior still operates under the linear region which means the above condition is met.

Regarding claim 10, AAPA discloses the photoelectric conversion device according to previous invention, wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor, said first switch and said second switch are field effect transistors, and different voltages are applied to gates of said first switch and said second switch.

Regarding claim 11, AAPA discloses the photoelectric conversion device according to previous invention, wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor and a second power supply line for supplying electric power of a voltage, different from the voltage

applied via said first power supply line, to said second switch, and said first switch and said second switch are field effect transistors.

Regarding claim 14, AAPA discloses the photoelectric conversion device wherein each of said pixel cell further comprises a second switch for resetting said gate area of said field effect transistor, and said first switch and said second switch are field effect transistors, and, when mobility is mu, capacitance of gate oxide per unit area is Cox, gate width is W, and gate length is L in said first switch, and K=1/2 * mu * Cox * W/L, a threshold voltage of said second switch is V.sub.th0, a threshold voltage of said first switch is V.sub.th1, the gate voltage of said second switch is V2, and the gate voltage of said first switch is V3, then, each pixel cell, inherently from the operation of the circuit because the structure of the claimed subject matter and the prior art is the same, satisfies a condition determined by

$$V3-Vth1-(Ia/K)^{1/2} > V2-Vth0-Vth$$

Regarding claim 18, AAPA discloses the photoelectric conversion device wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor, and said first switch and said second switch are field effect transistors, and, when mobility is .mu., capacitance of gate oxide per unit area is Cox, gate width is W, and gate length is L in said first switch, and K=1/2.times..mu..times.Cox.times.W/- L, a threshold voltage of said second switch is V.sub.th0, a threshold voltage of said first switch is V.sub.th1, the gate voltage of said second switch is V2, and the gate voltage of said first switch is V3, then, each pixel

cell, inherent from the operation of the circuit in Fig. 1, satisfies a condition determined by

V3-Vth1-(Ia/K+(V3-Vc1-Vth1)^2) ½ > V2 - Vth0 – Vth1.

Regarding claim 19, the photoelectric conversion device, wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor and a second power supply line for supplying electric power of a voltage, different from the voltage applied via said first power supply line, and said first switch and said second switch are field
effect transistors, and, when mobility is .mu., capacitance of gate oxide per unit area is Cox, gate width is W, and gate length is L in said first switch, and K=1/2 * mu * Cox *W/- L, a threshold voltage of said second switch is V.sub.th0, a threshold voltage of said first switch is V.sub.th1, the gate voltage of said second switch is V2, the gate voltage of said first switch is V3, and the voltage applied via said second power supply line is V.sub.c2, then, each pixel cell, inherent from the operation of the circuit shown in Fig. 1, satisfies a condition determined by

V3-Vth1- (Ia/K^1/2 > Vc2 - Vth where Vc2 <= V2-Vth0.

Regarding claim 20, the photoelectric conversion device according to claim 1, wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor and a second power supply line for supplying

electric power of a voltage, different from the voltage applied via said first power supply line, and said first switch and said second switch are field effect transistors, and, when mobility is .mu., capacitance of gate oxide per unit area is Cox, gate width is W, and gate length is L in said first switch, and

K=1/2 * mu * Cox * W/- L, a threshold voltage of said second switch is V.sub.th0, a threshold voltage of said first switch is V.sub.th1, the gate voltage of said second switch is V2, the gate voltage of said first switch is V3, and the voltage applied via said second power supply line is V.sub.c2, then, each pixel cell, inherent from the operation of the circuit shown in Fig. 1, satisfies a condition determined by

V3-Vth1-(Ia/K+(V 3-Vc1-Vth1)^2)^1/2 > Vc2-Vth where Vc2 <= V2 - Vth0

Allowable Subject Matter

Claims 2-9, and 12,13, 15-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art discloses the invention set forth above, prior does not disclose intentionally having the transistors threshold voltage different nor does the prior art disclose the gate voltage of the field effect transistor is controlled via a capacitor formed between the second switch and the gate area. Prior art does not disclose the photoelectric conversion device wherein each of said pixel cells further comprises a second switch for resetting said gate area of said field effect transistor and a third switch connected

between said photoelectric conversion element and an intersection of said second switch and the gate area of said field effect transistor, and capacitance of the gate area of said field effect transistor is set lower than capacitance of said photoelectric conversion element.

Prior art does not disclose voltage V2 of said second switch and the gate voltage V3 of said first switch are controlled to be equal, and the threshold voltage Vth of said field effect transistor, the threshold voltage Vth0 of said second switch and the threshold voltage Vth1 of said first switch are set to be equal, or voltage V2 of said second switch and the gate voltage V3 of said first switch are controlled equal, and the threshold voltage Vth0 of said second switch is set different from the threshold voltage Vth1 of said first switch are set equal, or voltage V2 of said second switch is controlled to be different from the gate voltage V3 of said first switch, and the threshold voltage Vth0 of said second switch is set different from the threshold voltage Vth1 of said first switch are set equal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony Ko whose telephone number is 571-272-1926. The examiner can normally be reached on Monday-Friday 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKo

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